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1) Where does the comparison level occur for 16-bit contents in the compare mode operation?

- a. Between CCPR1 register & TMR1
- b. Between CCPR1 & CCPR2 registers
- c. Between CCPR2 register & TMR1
- d. Between CCPR2 register & TMR0

**ANSWER: (a) Between CCPR1 register & TMR1**

2) Why are the pulse width modulated outputs required in most of the applications?

- a. To control average value of an input variables
- b. To control average value of output variables
- c. Both a & b
- d. None of the above

**ANSWER: (b) To control average value of output variables**

3) What would be the resolution value if oscillator and PWM frequencies are 16MHz and 2 MHz respectively?

- a. 2
- b. 3
- c. 4
- d. 8

**ANSWER: (b) 3**

4) How do the variations in an average value get affected by PWM period?

- a. Longer the PWM period, faster will be the variation in an average value
- b. Shorter the PWM period, faster will be the variation in an average value
- c. Shorter the PWM period, slower will be the variation in an average value
- d. Longer the PWM period, slower will be the variation in an average value

**ANSWER: (b) Shorter the PWM period, faster will be the variation in an average value**

5) Which among the below stated components should be filtered for determining the cut-off frequency corresponding to the PW period of low-pass filter?

- a. Fundamental  $F_{PWM}$  & higher harmonics
- b. Resonant  $F_{PWM}$  & higher harmonics
- c. Slowly Varying DC components
- d. Slowly Varying AC components

**ANSWER: (a) Fundamental  $F_{PWM}$  & higher harmonics**

**6) Which among the below stated conditions are selected by the SSPCON & SSPSTAT control bits?**

- a. Slave Select mode in slave mode
- b. Data input sample phase
- c. Clock Rate in master mode
- d. All of the above

**ANSWER: (d) All of the above**

**7) Which bit of SSPCON must be necessarily set so as to enable the synchronization of serial port?**

- a. WCOL
- b. SSPOV
- c. CKP
- d. SSPEN

**ANSWER: (d) SSPEN**

**8) What should be the value of SSPM3:SSPM0 bits so that SPI can enter the slave mode by enabling SS pin control?**

- a. 0000
- b. 0100
- c. 0010
- d. 0001

**ANSWER: (b) 0100**

**9) Which bits assist in determining the I<sup>2</sup>C bit rate during the initialization process of MSSP module in I<sup>2</sup>C mode?**

- a. SSPADD
- b. SSPBUF
- c. Both a & b
- d. None of the above

**ANSWER: (a) SSPADD**

**10) Which command/s should be essentially written for I<sup>2</sup>C input threshold selection and slew rate control operations?**

- a. SSPSTAT
- b. SSPIF
- c. ACKSTAT
- d. All of the above

**ANSWER: (a) SSPSTAT**

